In the Claims

CLAIMS

Claims 1-39 (Canceled).

40. (Previously presented) A semiconductor processing method comprising:

forming a conductive word line over at least a portion of a substrate active area, the word line having a conductive top;

forming nitride material over the conductive top of the word line;

forming sidewall spacers laterally adjacent to the word line, the sidewall spacers comprising a nitride;

forming an oxide material over the conductive word line and the substrate active area; and

etching the oxide material, the nitride material and the sidewall spacers at substantially the same rate, the etching outwardly exposing at least one portion of the substrate active area into which p-type impurity is to be provided, the etching also forming a contact opening over a portion of the conductive word line which overlies a field isolation region.

41. (Previously presented) The method of claim 40 further comprising doping the at least one portion of the substrate active area by ion implantation.

42. (Previously presented) The method of claim 40 further comprising doping the at least one portion of the substrate active area by gas chemical diffusion.

43. (Previously presented) The method of claim 40, wherein the etching defines a doping window through which the at least one portion of the substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening.

44. (Previously presented) The method of claim 40, wherein the etching defines a doping window through which the at least one portion of the substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening and further comprising angle doping the exposed at least one portion of the substrate active area to form source/drain regions.

45. (Previously presented) A semiconductor processing method comprising:

forming at least one conductive gate line comprising silicide over a substrate and extending over a substrate active area;

forming a nitride material over the silicide material;

forming oxide material over the at least one conductive gate line and the substrate active area; and

etching to remove portions of the nitride material over the conductive gate line to form a contact opening thereto and to remove portions of the oxide material over the substrate active area to expose source/drain regions into which p-type impurity is to be provided, the etching removing the nitride material and the oxide material at substantially the same rate.

46. (Previously presented) The method of claim 45, wherein the etching defines a doping window through which the substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening.

47. (Previously presented) The method of claim 45, wherein the etching defines a doping window through which the substrate active area is exposed, the doping window having a greater lateral width dimension than the contact opening and further comprising angle doping the exposed substrate active area to form the source/drain regions.

48. (Previously presented) A semiconductor processing method comprising:

forming a conductive line over a substrate, the conductive line having a conductive portion and silicon nitride material over the conductive portion, and silicon oxide material over the silicon nitride material;

forming encapsulation material over the conductive line; and

in a common masking step, etching a doping window opening over a substrate active area adjacent the conductive line and removing at least some of the encapsulation material over the conductive line and some of the silicon nitride material over the conductive portion of the conductive line to form a contact opening to the conductive line.

49. (Previously presented) The method of claim 48 further comprising gas diffusion doping through the doping window opening into the substrate active area with a p-type impurity.

50. (Currently amended) A semiconductor processing method comprising:

forming a conductive word line over a substrate;

forming a silicon nitride layer over the word line;

forming a silicon oxide layer over the silicon nitride layer;

forming encapsulation material over the silicon oxide layer, the silicon nitride layer and the conductive word line, the encapsulation material forming sidewall spacers over the conductive word line;

selectively removing at least some of the encapsulation material relative to the silicon oxide layer; and

selectively removing at least some of the silicon oxide layer relative to the silicon nitride layer wherein the selectively removing forms at least part of a contact opening over the word line.

51. (Previously presented) A semiconductor PMOS processing method comprising:

forming at least one conductive gate line having a conductive line top;

forming a nitride material over at least a portion of the conductive line top;

forming oxide material over the nitride material;

forming photoresist material over the oxide material;

in a common masking step, patterning the photoresist material to form a contact opening pattern configured for forming a contact opening over the conductive gate line and a doping window pattern over an active area of the substrate adjacent the conductive gate line, the contact opening pattern and the doping window pattern having respective lateral width dimensions, the contact opening pattern lateral width dimension being less than the doping window pattern lateral width dimension;

anisotropically etching both the nitride material and the oxide material at substantially the same rate to respectively define the contact opening to the conductive gate line and the doping window over the substrate active area adjacent the gate line; and

doping selected areas of the substrate active area with a p-type impurity to form at least a portion of one source/drain region.

52. (Previously presented) The method of claim 51 further comprising forming NMOS circuitry over the substrate, the PMOS circuitry and the NMOS circuitry collectively defining CMOS circuitry.

53. (Previously presented) A semiconductor processing method comprising:

forming at least one conductive gate line at least partially overlying a field isolation region and having a conductive line top;

forming a nitride material over at least a portion of the conductive line top;

forming an oxide material over the nitride material; and

using a common mask, etching both the nitride material and the oxide material at substantially the same rate to respectively form a contact opening over the conductive gate line and a doping window over an active area of a substrate adjacent the conductive gate line, wherein the common mask comprises contact opening pattern width dimension less than a doping window pattern width dimension.

54. (Previously presented) The method of claim 53 further comprising doping through the doping window into the active area of the substrate by ion implantation.

55. (Previously presented) The method of claim 53 further comprising doping through the doping window into the active area of the substrate by gas chemical diffusion.

56. (New) The method of claim 48, wherein the etching of the doping window opening comprises forming a pair of doping window openings adjacent opposite sides of the conductive line.

57. (New) The method of claim 48, wherein the etching comprises exposing the conductive portion of the conductive line.

58. (New) The method of claim 48, wherein the encapsulation material comprises nitride material.

59. (New) The method of claim 48, wherein the encapsulation material comprises material other than oxide material.

60. (New) The method of claim 48, wherein the forming of the encapsulation material comprises forming after the forming of the conductive line.

61. (New) The method of claim 48, wherein the encapsulation material and the silicon oxide material comprise different materials.

62. (New) The method of claim 50, wherein the encapsulation material comprises nitride material.

63. (New) The method of claim 50, wherein the forming of the encapsulation material comprises forming a substantial portion of the encapsulation material elevationally below the silicon oxide layer.